TEQIP SUMMER INTERNSHIP REPORT

THERMOMECHANICAL STRESS AWARE ON 3D IC

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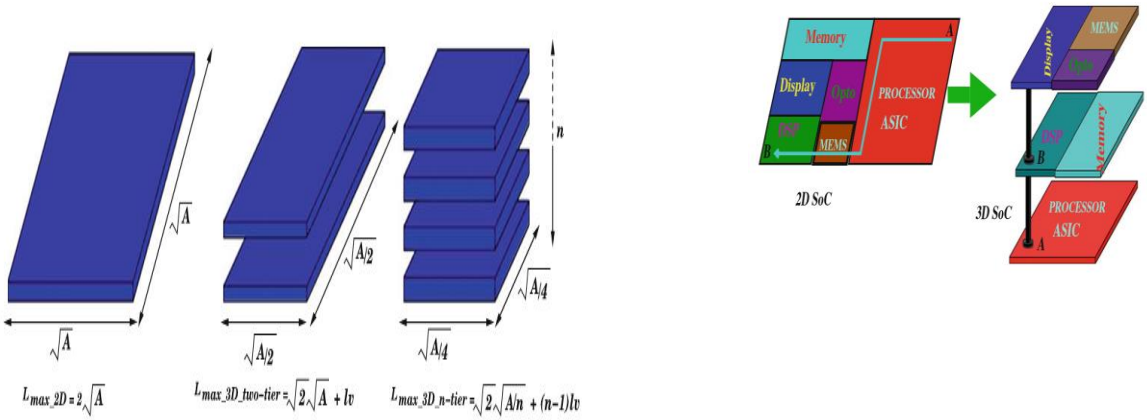
3D IC

Three-dimensional integrated circuits (3D-ICs), which contain multiple layers of active devices, have the potential to dramatically enhance chip performance, functionality, and device packing density. They also provide for microchip architecture and may facilitate the integration of heterogeneous materials, devices, and signals and offer a promising solution for reducing both silicon footprint and interconnect length without shrinking the transistors.

ADVANTAGE OF 3D IC

The main advantage of 3D IC is that, the interconnection wire length reduces, hence the propagation delays reduces.



Difference in wirelength between 2D SoC and 3D Soc.

CONCERNS IN 3D IC

3D IC has two main issues: reliability issues and thermomechanical stress. The thermomechanical stress has been considered as one of the most challenging in 3D IC designing due to the difference in thermal expansion coefficient between TSV and substrate layer.

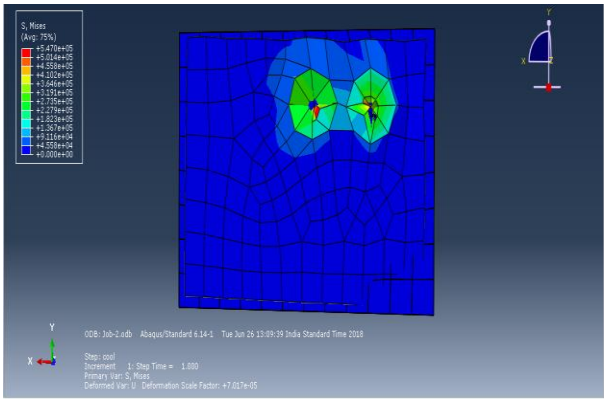
In this work it has been demonstrated that, how the TSV or substrate layer deform when it is subjected to thermal stress. To demonstrate the thermal stress analysis ABAQUS tool is used.

STRESS MODELLING

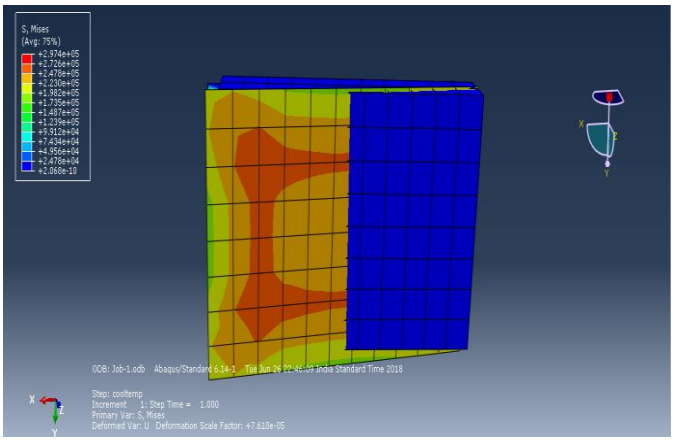
The intrinsic stress occurs whenever a small external force is applied. The extrinsic forces are classified under two categories: Layout dependent and Layout independent, these two stresses are analysed separately and then added to get the total stress.

LAYOUT DEPENDENT: It is induced by the stress sources related to layout, specifically stresses caused by the locations of the TSVs and μ-bumps relative to various blocks in the layout.

Modelling: To model the layout dependent stress, the 3D stacked layers with TSV are subjected to a thermal stress of 275^{o}c .The material property and the CTE(coefficient of thermal expansion) are specified.



Stacked layer with TSV subjected to a thermal stress of 275^{o}c.(layout dependent)



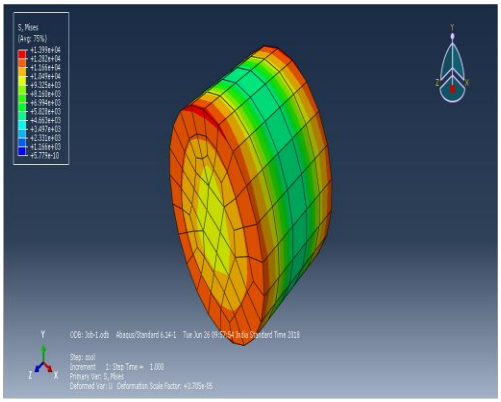
Layer without TSV, under a thermal stress of 400^{o}c (Layout independent)

LAYOUT INDEPENDENT STRESS: It does not vary with the layout: here, this corresponds to warpage caused by the CTE mismatch between layers. Intrinsic stress is also layout-independent.

Modelling: To model the layout independent stress, the layers are stacked without TSV and are subjected to a thermal stress of around 400^{o}c.

Dimensions

	Diameter	Height	Pitch
TSV	20µm	50µm	25µm



Single TSV under the thermal stress of 275^{o}c

Material parameters

Materials	CTE(ppm/K)	Young's Modulus (GPa)	Poisson ratio
Si	2.3	188	0.27
Cu	17	110	0.35
Sio2	0.5	71	0.17
Substrate	17.6	19.7	0.13

Experimental results: In the work, for single TSV and two stacked layer, the thermal stress has been analysed. From the simulation, it has been observed that under the thermal stress the mobility and the threshold voltage of the IC changes.

Conclusion: 3-Dimensional Integrated Circuit provides high speed computation with low power consumption. However several reliability issues still exists in the 3D IC caused by the TSV, µ bump, layer stacking. In this work, the thermomechanical stress induced in the 3D IC were evaluated by the tool (ABAQUS 6.14). Using these evaluation methods the design guidelines of 3D IC can be optimized and highly reliable 3D IC can be fabricated.

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